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PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Enable PCIe and USB 3.0 on M.2 Card Key B
DATE:	September 2, 2016
AFFECTED DOCUMENT:	PCI Express M.2 Specification, Revision 1.1
SPONSOR:	Jim Panian, Qualcomm Technologies Inc.

Part I

1. Summary of the Functional Changes

M.2 Key B (WWAN) is modified to enable PCIe and USB 3.0 signals to be simultaneously present on the connector. This enables support for a single SKU M.2 card that supports both PCIe and USB 3.0. There are two implementation options enabled:

1. State #14 in the "Socket 2 Module Configuration Table" is re-defined to indicate a module built to Revision 1.1 or later where both PCIe and USB 3.0 are both present on the connector. The choice of Port Configuration is vendor defined. This enables the host to unambiguously determine that PCIe and USB 3.0 are present on the connector.

2. States #4, 5, 6, 7 in the "Socket 2 Module Configuration Table" are re-defined to indicate that in addition to USB 3.0, PCIe may be present on the connector. This definition is used by M.2 cards built to Revision 1.0 or later (USB 3.0 on connector; PCIe is "no connect"). This definition is also permitted to be used by M.2 cards built to Revision 1.1 or later to indicate that PCIe and USB 3.0 are both present on the connector. This allows GPIO port configurations to remain consistent with all other existing states.

2. Benefits as a Result of the Changes

An M.2 card as a single SKU may be designed for insertion into a:

- Host system that only supports PCIe
- Host system that only supports USB 3.0
- Host system that supports PCIe and/or USB 3.0

3. Assessment of the Impact

This feature is optional. It will have no impact on existing implementations.

4. Analysis of the Hardware Implications

Hardware changes are required to take advantage of this new optional capability.

5. Analysis of the Software Implications

None.

6. Analysis of the C&I Test Implications

None.

Part II

Detailed Description of the changes

Update Table 29, Socket 2 Module Configuration, page 155 as follows:

Table 29. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
`	GND	N/C	GND	GND	SSD – PCIe	N/A
2	GND	GND	N/C	GND	WWAN – PCIe	0
3	GND	N/C	N/C	GND	WWAN – PCIe	1
4	GND	GND	GND	N/C	WWAN – PCIe, USB3.0	0[4,5]
5	GND	N/C	GND	N/C	WWAN – PCIe, USB3.0	1[4,5]
6	GND	GND	N/C	N/C	WWAN – PCIe, USB3.0	2[4,5]
7	GND	N/C	N/C	N/C	WWAN – PCIe, USB3.0	3[4,5]
8	N/C	GND	GND	GND	WWAN – SSIC	0
9	N/C	N/C	GND	GND	WWAN – SSIC	1
10	N/C	GND	N/C	GND	WWAN – SSIC	2
11	N/C	N/C	N/C	GND	WWAN – SSIC	3
12	N/C	GND	GND	N/C	WWAN – PCIe	2
13	N/C	N/C	GND	N/C	WWAN – PCIe	3
~~14~~	~~N/C~~	~~GND~~	~~N/C~~	~~N/C~~	~~RFU~~	~~N/A~~
14	N/C	GND	N/C	N/C	WWAN – PCIe, USB3.0	Vendor Defined [3,5]
15	N/C	N/C	N/C	N/C	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3).

[2] Applicable to WWAN only.

[3] Permitted for use by a module built to Revision 1.1 or later where PCIe and USB3.0 are both present on the connector. Vendor defined choice of port configurations 0,1,2,3. Refer to Table 33.

[4] Used by a module built to Revision 1.0 or later where USB3.0 is present on the connector and PCIe is no-connect. Refer to Table 31. Permitted for use by a module built to Revision 1.1 or later where PCIe and USB3.0 are both present on the connector. Refer to Table 33.

[5] Only a single lane of PCIe is available in these states.

Add a new table after Table 32, page 159 as follows:

Table 33. Socket 2 Key B PCIe/USB3.0-based WWAN Module Pinout

3.3V	CONFIG_2 (States 4,5,6,7 and 14)
3.3V	GND
3.3V	GND
SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 4,5,6,7 and 14)
SIM_DETECT (I)	RESET# (I)(0/1.8V)
COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)
COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)
COEX3(I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)
N/C	ANTCTL0 (O)(0/1.8V)
N/C	GND
PEWAKE# (I/O)(0/3.3V)	REFCLKp
CLKREQ# (I/O)(0/3.3V)	REFCLKn
PERST# (I)(0/3.3V)	GND
VENDOR DEFINED or GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERp0
VENDOR DEFINED or GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	PERn0
VENDOR DEFINED or GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	GND
VENDOR DEFINED or GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DTA2/IPC_1 (I/O)(0/1.8V*)	PETp0
VENDOR DEFINED or GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	PETn0
N/C	GND
UIM-PWR (O)	USB3.0-Rx+
UIM-DATA (I/O)	USB3.0-Rx-
UIM-CLK (O)	GND
UIM-RESET (O)	USB3.0-Tx+
VENDOR DEFINED or GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	USB3.0-Tx-
VENDOR DEFINED or GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	GND
VENDOR DEFINED or GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	DPR (I)(0/1.8V)
VENDOR DEFINED or GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	VENDOR DEFINED or GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)
VENDOR DEFINED or GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 (States 4,5,6,7 and 14)
Module Key	Module Key
Module Key	Module Key
Module Key	Module Key
Module Key	Module Key
VENDOR DEFINED or GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND
W_DISABLE1# (I)(0/3.3V)	USB_D-
FULL_CARD_POWER_OFF# (I)(0/1.8V)	USB_D+
3.3V	GND
3.3V	GND
	CONFIG_3 (States 4,5,6,7 and 14)

Update Section 5.2.1, page 191, as follows:

5.2.1 Socket 2 Module Key B

5.2.1.1 Socket 2 Module Key B – Configuration Pin Definitions

The Socket 2 Key (Mechanical Key B) is unique in that it enables five major pinouts configurations and four variants for each of the three WWAN configurations. The five major configurations supported are:

WWAN that is PCIe Based

WWAN that is SSIC Based

WWAN that is USB3.0 or PCIe/USB3.0 Based

SSD that is PCIe (2 lane) Based

SSD that is SATA Based

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Update Table 51, page 192 as follows:

Table 51. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - PCIe,USB3.0	0[4,5]
0	1	0	1	WWAN - PCIe,USB3.0	1[4,5]
0	0	1	1	WWAN - PCIe,USB3.0	2[4,5]
0	1	1	1	WWAN - PCIe,USB3.0	3[4,5]
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3
~~1~~	~~0~~	~~1~~	~~1~~	~~RFU~~	~~N/A~~
1	0	1	1	WWAN – PCIe,USB3.0	Vendor Defined[3,5]
1	1	1	1	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3).
[2] Applicable to WWAN only.
[3] Permitted for use by a module built to Revision 1.1 or later where PCIe and USB3.0 are both present on the connector. Vendor defined choice of port configurations 0,1,2,3. Refer to Table 33.
[4] Used by a module built to Revision 1.0 or later where USB3.0 is present on the connector and PCIe is no-connect. Refer to Table 31. Permitted for use by a module built to Revision 1.1 or later where PCIe and USB3.0 are both present on the connector. Refer to Table 33.
[5] Only a single lane of PCIe is available in these states.